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PATENT APPLICATION FULL TEXT AND IMAGE DATABASE



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Apparatus and method for an interface unit for data transfer between data processing units in the asynchronous transfer mode and in the I/O mode

Abstract

In a data processing system have a master-state data processing unit and at least one slave-state data processing unit, the data processing units can be provided with an asynchronous transfer mode interface unit for transferring data cells there between. The interface unit provides and receives signals formatted in the UTOPIA protocol. The interface unit includes processor acting as a state machine and a buffer out memory unit for buffering the data groups between the interface unit processor and the direct memory access unit of the data processing unit. The interface unit can act in a receive mode and a transmit mode for a master-state data processing unit and can act in a receive mode, and transmit mode in a slave-state data processing unit. An event signal provides an efficient exchange of transfer of data between the direct memory access unit and the buffer memory storage unit in the slave mode. Through correct use of the signals exchanged with a communication bus, the UTOPIA ATM interface unit can function as an I/O unit.

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Claims

What is claimed is:

1. An interface unit controlling the exchange of signals between a data processing unit and a communication bus, the interface unit comprising: a receive channel for receiving data groups from the communication bus and the applying the data groups to the data processing unit; and a transmit channel for receiving data groups from the data processing unit and applying the signal groups to a communication bus, wherein the interface unit can function in an ATM interface mode and can function in an I/O interface mode.
2. The interface unit as recited in claim 1 wherein the interface unit can function is a UTOPIA ATM interface mode and can function in an I/O interface mode.
3. The interface unit as recited in claim 1 wherein the interface unit exchanges data groups with the direct memory access unit of the data processing unit.
4. The interface unit as recited in claim 1 further comprising a control register, the control register determining when the interface unit is in the ATM mode of operations and when the interface unit is in the I/O mode of operation.
5. The interface unit as recited in claim 1 wherein the interface unit includes: an input interface unit; an output interface unit; an input buffer memory unit, wherein the transfer between the input buffer memory unit and the direct memory access unit is determined by a receive event signal; and an output buffer memory unit, wherein the transfer between the direct memory access unit and the output buffer memory unit is determined by a transmit event signal.
6. The interface unit as recited in claim 1 wherein the UTOPIA ATM URDATA signal corresponds to an I/O OUTDATAVALID signal, and wherein a UTOPIA ATM UXCLAV signal corresponds to an I/O INDATAVALID signal.
7. A method of exchanging data groups between a communication bus and a data processing system, the method comprising: in response to a first set of signals in an interface unit, exchanging data groups in a ATM mode of operation; and in response to a second set of signals in the interface unit, exchanging data groups in an I/O mode of operation.
8. The method as recited in claim 7 wherein exchanging data groups includes exchanging data groups in a UTOPIA AMT mode of operation.
9. The method as recited in claim 8 wherein the processor is a digital signal processor.
10. The method as recited in claim 8 further comprising implementing the interface unit including: an input interface unit; an output interface unit; an input buffer memory unit, wherein the transfer between the input buffer memory unit and the direct memory access unit is determined by a receive event signal; and an output buffer memory unit, wherein the transfer between the direct memory access unit and the output buffer memory unit is determined by a transmit event signal.

11. The method as recited in claim 10 further including storing the first and the second set of signals in a control register in the interface unit.

12. The method as recited in claim 11 wherein the UTOPIA ATM URDATA signal corresponds to an I/O OUTDATAVALID signal, and wherein a UTOPIA ATM UXCLAV signal corresponds to an I/O INDATAVALID signal.

13. A data processing unit comprising: a connector for coupling to a communication bus; a processor; and an interface unit implementing the exchange of data groups between the connector and the processor; the interface unit including a control register, the interface unit operating in an ATM mode when a first set of signals are stored in the control register, the interface unit operating in an I/O mode when a second set of signals are stored in the control register.

14. The data processing system as recited in claim 13 wherein the interface unit operates in a UTOPIA ATM mode when the first set of signals are stored in the control register.

15. The interface unit as recited in claim 13, the interface unit including: an input interface unit; an output interface unit; an input buffer memory unit; wherein the transfer between the input buffer memory unit and the direct memory access unit is determined by a receive event signal; and an output buffer memory unit, wherein the transfer between the direct memory access unit and the output buffer memory unit is determined by a transmit event signal.

16. The data processing unit as recited in claim 13 wherein the processor includes a direct memory access unit, the interface unit coupled between the direct memory access unit and the connector.

17. The data processing unit as recited in claim 13 wherein the UTOPIA ATM URDATA signal corresponds to an I/O OUTDATAVALID signal, and wherein a UTOPIA ATM UXCLAV signal corresponds to an I/O INDATAVALID signal.

Description

[0001] This application claims priority under 35 USC 119(e)(1) of Provisional Application Serial Number 60/237,237, filed Oct. 02, 2000.

RELATED APPLICATIONS

[0002] APPARATUS AND METHOD FOR AN INTERFACE UNIT FOR DATA TRANSFER BETWEEN PROCESSING UNITS IN THE ASYNCHRONOUS TRANSFER MODE; U.S. patent application No. (Attorney Docket No. TI-31779); filed on even date herewith; invented by Shakuntala Anjanaiah and Natarajan Seshan; and assigned to the assignee of the present application: APPARATUS AND METHOD FOR AN INTERFACE UNIT FOR DATA TRANSFER BETWEEN A HOST PROCESSING AND A MULTI-TARGET DIGITAL SIGNAL PROCESSING IN AN ASYNCHRONOUS TRANSFER MODE; U.S. patent application No. (Attorney Docket No. TI-33430); filed on even date herewith; invented by Martin Li, Jay Reimer Shakuntala Anjanaiah, Natarajan Seshan and Patrick Smith; and assigned to the assignee of the present application: and APPARATUS AND METHOD FOR INPUT CLOCK SIGNAL DETECTION IN AN ASYNCHRONOUS TRANSFER MODE INTERFACE UNIT; U.S. patent application No. (Attorney Docket No. TI-33533); filed on even date herewith; invented by Shakuntala Anjanaiah; and assigned to the assignee of the present application are related applications.

BACKGROUND OF THE INVENTION

[0003] 1. Field of the Invention

[0004] This invention relates generally to data processing systems and, more particularly, to data processing systems having a host processor and at least one digital signal processor. An interface unit is inserted between the host processor and the digital signal processor(s) to facilitate the exchange of data there between.

[0005] 2. Background of the Invention

[0006] As the requirements for computational power have increased, one data processing system that has been increasingly employed to meet these requirements includes a host processing system that controls one or more digital signal processors. The host processor is typically a microprocessor, but can be a digital signal processor. The host processor has the flexibility to respond to a wide variety of conditions and provide an appropriate response. The digital signal processors provide specialized capabilities that permit complex but repetitive tasks to be performed very rapidly. Thus, one or more digital signal processing units, operating under control of a master processing unit, can respond to a wide variety of computational intensive requirements. However, the host processor and the digital signal processor(s) may not be directly compatible and may even be fabricated by different manufacturers. In order to permit the interchange of data between incompatible components or components which can exchange data with difficulty, standard signal protocols have been agreed upon to provide the requisite commonality. As an example, the asynchronous transfer mode defines signals that facilitate the exchange of data signal groups between a host processor and a digital signal processor. A protocol has been provided for the Universal Test and Operations Phy Interface (UTOPIA) for the asynchronous transfer mode (ATM) (UTOPIA) Level 2 Interface to conform to the ATM Forum standard specification af-phy-0039.000 as well as other applicable standards. The UTOPIA protocol defines the interface between the Physical Layer (PHY) and the upper layer module such as the ATM Layer and various management entities. This definition allows a common PHY in ATM systems across a wide range of speeds and media types. The ATM cell or packet that is transferred in this protocol includes 53 bytes with a 5 byte header and a 48 byte payload in an 8-bit transfer mode, or 54 bytes with a 6 byte header and a 48 byte payload in a 16-bit transfer mode.

[0007] The UTOPIA protocol defines the exchange of data signals between master processing unit and the slave processing unit. An interface unit must be provided to buffer the data that are typically exchanged between a (relatively low-speed) communication bus and a direct memory access unit associated with the digital processing unit. In addition, to the transmit and receive functions that must be performed by the interface unit, a common configuration requires that one of the processing unit of the system operate in a master state while one or more processing units coupled thereto have a slave status.

[0008] The asynchronous transfer mode interface unit is only one of the possible devices that can provide an interface between a digital signal processing unit and other data processing devices. Another interface device is the I/O interface unit. In fabricating a chip, the device can include one type of interface unit or both types of interface units. The inclusion of only one type of interface unit limits the utility of the chip. The inclusion of both types of interface units on a chip increases the both the size and the complexity of the chip design.

[0009] A need has therefore been felt for apparatus and an associated method having the feature that an integrated circuit chip with a digital signal processing unit can include the functionality of an I/O interface unit and a ATM interface unit. It is another feature of the present apparatus and associated

method to provide an interface unit for an integrated circuit digital signal processing unit that can operate in the ATM mode or in the I/O interface unit mode. It is a more particular feature of the apparatus and associated method to provide an interface unit the can operate in the UTOPIA ATM mode or in the I/O mode.

SUMMARY OF THE INVENTION

[0010] The aforementioned and other features can be accomplished, according to the present invention, by providing a digital signal processor configuration with an interface unit responsive to UTOPIA-defined signals. The UTOPIA interface unit is a generalized interface unit that provides UTOPIA-defined signal set to external apparatus and responds to the UTOPIA-defined signal set from an external apparatus. The interface unit exchanges signals between the direct memory access unit of the data processing unit of which the interface unit is a component and a communication bus. The signals exchanged between the interface unit and the communication buses are implemented to provide efficient transfer of data there between. In particular, the interface unit can exchange data cells continuously with a communication bus. The interface unit includes a processor (acting as a state machine) for receiving and generating signals and buffer memory unit for buffering the flow data. The interface unit can operate in a master state with both a transmit mode and a receive mode and can operate in a slave state in both a transmit and receive mode. The interface unit can operate not only in the UTOPIA ATM interface mode but also in the I/O mode with the proper interpretation of the interface signals.

[0011] Other features and advantages of present invention will be more clearly understood upon reading of the following description and the accompanying drawings and the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. 1 is a block diagram of the general data processing system capable of advantageously using the present invention.

[0013] FIG. 2 is a block diagram illustrating the signals generated by and signals received by the asynchronous transfer mode interface unit in the slave-transmit state according to the present invention.

[0014] FIG. 3 is a timing diagram for the signals received by and generated by the asynchronous transfer mode interface unit in the slave-transmit state shown in FIG. 2 according to the present invention.

[0015] FIG. 4 is a block diagram illustrating the signals generated by and received by the asynchronous transfer mode interface unit in the slave-receive state according to the present invention.

[0016] FIG. 5 a timing diagram for the signals received by and generated by the asynchronous transfer mode interface unit in the slave-receive state mode shown in FIG. 4 according to the present invention.

[0017] FIG. 6 is a block diagram illustrating the signals generated by and received by the asynchronous transfer mode interface unit in the master-transmit state according to the present invention.

[0018] FIG. 7 is a timing diagram for the signals received by and generated by the asynchronous transfer mode interface unit in the master-transmit state mode shown in FIG. 6 according to the present invention.

[0019] FIG. 8 is a block diagram illustrating the signals generated by and received by the asynchronous transfer mode interface unit in the master-receive state according to the present invention.

[0020] FIG. 9 is a timing diagram for the signals received by and generated by the asynchronous transfer mode interface unit in the slave-receive state mode shown in FIG. 8 according to the present invention.

[0021] FIG. 10A illustrates the asynchronous transfer mode Utopia protocol signals with a master-state data processing unit in a transmit mode and a plurality of slave-state data processing units in a receive mode, while FIG. 10B illustrates the asynchronous transfer mode Utopia protocol signals with a master-state data processing unit in a receive mode and a plurality of slave-state data processing units in a transmit mode.

[0022] FIG. 11 is a block diagram of an implementation of the Utopia interface unit according to the present invention

[0023] FIG. 12 illustrates the contents of the interface control register according to the present invention

[0024] FIG. 13 is a flow chart illustrating the operation of an EVENT signal in the Utopia interface slave transmit mode according to present invention.

[0025] FIG. 14 is a flow chart illustrating the operation of an EVENT signal in the Utopia interface slave receive mode.

[0026] FIG. 15 illustrates the connection between a Utopia protocol interface unit in the slave mode to an exemplary digital signal processing unit according to the present invention.

[0027] FIG. 16A is a timing diagram for the for the Utopia interface unit acting in the slave transmit I/O mode according to the present invention, while FIG. 16B is a timing diagram for Utopia interface unit acting in the slave receive I/O mode according to the present invention

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0028] 1. Detailed Description of the Figures

[0029] Referring to FIG. 1, a block diagram of the data processing system 1 capable of advantageously incorporating the present invention is shown. The data processing system includes at least one digital signal processing unit 100 through 10N, a communication bus 110, and a master processing unit 120. Each digital signal processing unit 100 through 10N includes a central processing unit (or digital signal processing unit core) 10, memory unit 12, a direct memory access unit 14, and a UTOPIA interface unit 18. The interface unit 18 of each digital signal processing unit 100 through 10N exchanges signals with the bus 100. Master processing unit 120 also exchanges signals with the communication bus 110. The interface unit 18 exchanges signals with the direct memory access unit 14. The direct memory access unit 14 exchanges signals with the memory unit 12 and, subsequently, with the core processing unit 10. Note that the master processing unit 120 can be digital processing unit such digital signal processing unit 100.

[0030] Referring to Table 1, the required signals for the ATM Forum Technical Committee's UTOPIA Level 2, Version 1.0 (af-phy-0039.000) are listed. Note that optional signals, not included in Table 1, are identified.

1 TABLE 1 ATM Controller ATM Controller Master Slave Signal Name (Dir) (Dir) Transmission Mode UXCLK In In UXADDR {4:0} Out In UXCLAV In Out UXENB Out In UXSOC Out Out UXDATA {15:0} Out Out Receive Mode URCLK In In URADDR {4:0} Out In URCLAV In Out URENB Out In URSOC In In URDATA {15:0} In In

[0031] In the transmit slave mode, the Utopia signals have the following meaning. The UXCLK signal is a clock input signal driven by the master processing unit. The UXDATA signals and the transmit control signals are synchronized with this UXCLK signal. The UXADDR {4:0} is 5-bit address signal group generated by the master processing unit. This address signal group is used to select one of a plurality (up to 31) slave processing units in the system. The UXCLAV signal is a transmit cell available status output signal of the slave processing unit. For a cell level handshake, a 0 logic level indicates that the slave interface unit does not have a complete data cell for transmission, while a logic 1 indicates that the slave interface unit has a complete data cell to transmit. The UXENB signal is a transmit interface enable signal input signal. This signal is asserted low by the master processing unit to indicate that the slave processing unit should apply the first byte of valid data and the UXSOC (start-of-cell) signal in the next clock cycle. The UXSOC signal is the start of cell signal (active high) that is generated by the slave processing unit on the rising edge of the UXCLK signal to indicate that the first valid byte of the cell is available on the transmit data bus. The UXDATA {15:0} signals are provided by the slave processing unit during the transmission of on the transmit data bus on the UXCLK rising edge.

[0032] In the receive slave mode, the URCLK signal is a clock signal applied to the interface unit by the master processing unit. The receive data and control signals are sampled and are synchronous to this clock signal. The URADDR {4:0} signals are applied to the interface unit by the master processor and identify one of the slave units (up to 31) in the system. The URCLAV signal is the receive cell available output signal from the slave interface unit to indicate that the slave interface unit has space available to receive a cell from the master processing unit. In the handshake procedure, the 0 logic bit indicates that no space is available to receive a data cell from the master processing unit. The 1 logic bit indicates that space is available to receive a data cell from the master processing unit. The URENB signal is an active low signal generated by the master processing unit to enable the receive interface of the slave processor. This signal indicates that the slave interface unit is to sample URDATA signal and the URSOC signal during the next clock cycle or thereafter. The URSOC signal is generated by the master processing unit and indicates that the first valid byte of the data cell is available on the receive data bus for the slave processor to sample. The URDATA {15:0} signals are applied by the master processor to the data receive bus and sampled on the rising edge of the CLK signal.

[0033] As can be seen from Table 1, in the master mode, the UXCLAV/URCLAV and the UXENB/URENB signals are reversed in direction when compared to the counterpart slave signals. The reversal in direction is the result of the different role played by a master mode interface unit and a slave mode interface unit. Similarly, the UXADDR and URADDR signals have reversed directions between the master mode and the slave mode resulting from the fact that the polling takes place from the master mode. The interpretation of the signals remains the same.

[0034] Referring to FIG. 2, the signals applied to and generated by the UTOPIA interface unit 18 in the slave transmit mode are shown. The interface unit 18 includes two components, a processor 184 acting as a state machine, and a buffer memory unit 182. The processor 184 receives the UXCLK signal, the UXADDR {4:0} signal and the UXENB signal. The processor 184 generates the UXCLAV signal, the UXSOC signal and the UXDATA {15:0} signal. The processor 184 applies the WRD_RDY signal to the buffer memory unit and the processor 184 receives the DATA {31:0} signals and the CLAV signal from the buffer memory unit 184. The buffer memory unit 182 receives the WD_WR signal, the ADDR {31:0} signals, the data {31:0} signals and the ADDR {31:0} signals from the direct memory access unit 14. The buffer memory unit 182 applies the EVENT signal to the direct memory access unit 14.

[0035] Referring to FIG. 3, a timing diagram illustrating the relationship of the signals for the asynchronous transfer mode interface unit 14 in the transmit-mode depicted in FIG. 2 are shown. The signals are synchronized by the UXCLK signal. When a slave mode asynchronous transfer mode

interface unit 18 detects its address on the UXADDR {4:0} lines, the processor will provide a UXCLAV signal to indicate whether or not a cell is available for transmission. After completion of the current activity, the master processor generates the address signal group, UXADDR {4:0}, and the UXENB signal. The slave processor then transmits the data over the conductors carrying the DATA {15:0} signals and by asserting the UXSOC signal.

[0036] Referring to FIG. 4, the exchange of signals between the interface unit 18 and the master processing unit and between the interface unit 18 and the direct memory access unit 14 is shown. The processor 184 of the interface unit 18 receives the URCLK signal, the URADDR {4:0} signals, the URENB signal, the URSOC signal, and the URDATA {15:0} signals from the master processing unit. The processor 184 applies the URCLAV to the master processing unit. The processor 184 applies the DATA {31:0} signals and the WD_WR to the buffer memory unit 182 and processor 184 receives the CLAV signal from the buffer memory unit 182. The buffer memory unit 182 applies the DATA {31:0} signals and the EVENT signal to the direct memory access unit 14 and the buffer memory unit 182 receives the ADDR {31:0} signals and the WD_RD signal from the direct memory access unit 14. In the slave receive mode, the DATA signals are transferred by the processor 184 to the buffer memory unit 182, and then to the direct memory access unit 14. The CLAV signal and the WD_WR signal permit the DATA signals to be transferred through the processor 184 to the buffer memory unit 182. The WD_RD signal permits the DATA signals to be transferred from the buffer memory unit 182 to the direct memory access unit 14.

[0037] Referring to FIG. 5, a timing diagram illustrating the relationship of the signals for the asynchronous transfer mode interface unit 14 in the receive-mode depicted in FIG. 4 are shown. The signals are synchronized by the URCLK signal. The master processor applies the ADDR {4:0} signal group to the slave processors. The identified slave processor responds to the ADDR {4:0} signal with the appropriate CLAV signal. When an active CLAV signal is applied, the ADDR {4:0} signals are reapplied along with the ENB signal. The slave starts receiving data along with an SOC signal. The DATA {15:0} signals continue to be received until the cell has been completely transferred.

[0038] Referring to FIG. 6, the signals exchanged by the interface unit 18 in the master-transmit mode is shown. The processor 184 of the interface unit 18 receives the UXCLK signal and the UXCLAV signal. The interface unit 184 applies the UXADDR [4:0] signals, the UXENB signal, the UXSOC signal, and the UXDATA {15:0} signals to the slave processing unit. The processor 184 applies the WD_RD signal to the buffer memory unit 182 and processor 184 receives the DATA {31:0} signals and the CLAV signals from the buffer memory unit 182. The buffer memory unit 182 applies the EVENT signal to the direct memory access unit 14 and the buffer memory unit 182 receives the DATA {31:0} signals, the ADDR {31:0} signals, and the WD_WR signal from the direct memory access unit 14. In the master-state transmit state the DATA signals are transmitted from the direct memory access unit 14 to the buffer out memory unit 182, and then through the processor 184 to the external component. The WD_WR signal permits the DATA signals to be transmitted from the direct memory access unit 14 to the buffer memory unit 182. The CLAV signal and the WR_RD signal permit the DATA signals to be transferred from the buffer memory unit 182 to the processor 184 and, subsequently to the external component.

[0039] Referring to FIG. 7, the timing diagram for the Utopia interface unit in the master-transmit state of FIG. 6 is shown. The master-transmit state processor polls, with the UXADDR {4:0} signals, the slave devices in a round robin or in a fixed priority sequence. The processor 184 receives a UXCLAV signal, where appropriate, from a slave processor following the address, UXADDR {4:0} of the processor. The master-transmit processor then reapplies the address of the slave processor generating the UXCLAV signal along with the UXENB signal. During the next clock cycle, the processor begins transmission of the UXDATA {15:0} signals and the SOC signals to the slave processor. The transfer is

continued until the entire cell has been transferred.

[0040] Referring to FIG. 8, the signals exchanged by the UTOPIA interface unit 18 in the master-receive mode are shown. The processor 184 of the interface unit 18 applies the URADDR {4:0} signals and the URENB signal to the slave processing unit and the processor 184 receives the URCLK signal, the URCLAV signal, the URSOC signal and the URDATA {15:0} signals from the slave processing unit. The processor 184 applies the DATA {31:0} signals and the WD_WR signals to the buffer memory unit 182 and the processor 184 receives the CLAV signal from the buffer memory unit 182. The buffer memory unit 182 applies the DATA {31:0} signals and the EVENT signal to the direct memory access unit 14 and the buffer memory unit 182 receives ADDR {31:0} signals and the WD_RD signal from the direct memory access unit 14.

[0041] Referring to FIG. 9, a timing diagram is shown for the signals of the asynchronous transfer mode interface unit in the master-receive state as illustrated in FIG. 8. The master processor 184 of polls the slave processors by applying the ADDR {4:0} signals to the address line. When a slave asynchronous transfer mode interface unit is available to receive the data signals, a CLAV signal is asserted during the next clock cycle. During the following clock cycle, the ADDR {4:0} signals of the slave unit generating the CLAV signal is reapplied to the bus along with the ENB signal. When a current interaction with the master processor is complete, the addressed slave processor transmits the DATA {31:0} signals and the SOC signal. The DATA {31:0} are transmitted until the entire cell has been transferred.

[0042] Referring to FIG. 10A and FIG. 10B, a data processing system is shown having a master-state data processing unit 91 and a plurality of slave-state data processing units 92A through 92N. In FIG. 10A, the master-state data processing unit 91 is in a transmit mode, while the slave-state data processing units 92A through 92N are in a receive mode. In FIG. 10B, the master-state data processing unit 91 is in a receive mode while the slave-state data processing units 92A through 92N are in a transmit mode. In FIG. 10A, the master data processing unit 91 (in the transmit mode) generates the UXCLK, the UXADDR, the UXENB, the UXSOC, and the UXDATA signals that which become the URCLK, the URADDR, the URENB, the URSOC, and the URDATA signals, respectively, when applied to the slave data processing units 92A-92N (in the receive mode). The URCLAV signals from the slave data processing units 92A-92N are applied to the master data processing unit 91 as the UXCLAV signal. In FIG. 10B, the master data processing unit 91 (in the receive mode) generates the URCLK, the URADDR, and the URENB signals that are applied to the slave data processing units 92A-92N (in the transmit mode) as the UXCLK, the UXADDR, and UXENB signal respectively. The slave data processing units 92A-92N generate the UXCLAV, the UXSOC, and the UXDATA signals that are applied to the master data processing unit 91 as the URCLAV, the URSOC, and the URDATA signals, respectively.

[0043] Referring to FIG. 11, the implementation of the UTOPIA interface unit between the communication bus 110 and the direct memory access unit 14, according to the present invention, is shown. Data from the communication bus 110 is transferred through the interface input unit 181 to the interface input buffer memory unit 182. From the interface input buffer memory unit 182, the data signals are transferred through the direct memory access unit 14 to the memory unit(s) of the digital signal processing unit chip 100. The data from the memory units is transferred through the direct memory access unit 14 to the interface output buffer memory unit 183. The data is transferred from the interface output buffer memory unit 183 through the interface output unit 184 to the communication bus 110. The system logic 186 receives the INTERNAL CLOCK signal (as distinguished from the UTOPIA CLK signal), reshapes and deskews waveform and distributes the CLOCK signal to the rest of the UTOPIA interface unit 18. The configuration interface unit 185 receives the initialization signals and, by transmission of control signals to the other units of the UTOPIA interface unit 18 determines the mode in which the UTOPIA interface unit 18 operates. These control signals are stored in the interface control

register 1851.

[0044] Referring to FIG. 12, the contents of the interface control register according to the preferred embodiment is shown. In the UREN/UXEN fields, a logic "0" indicates that the receive/transmit port is disabled, while a logic "1" indicates that the interface receive port is enabled. This designation is true in both the master and the slave modes. In the URMSTRIUXMSTR fields, a logic "0" indicates that the interface unit is operating in a slave (default) mode, while a logic "1" indicates that the interface unit is operating in a master mode. In the RUDC/XUDC fields, a user defined (i.e., standard or extended) data cell is specified for both the receive and the transmit operational modes. This field is used in the slave mode. In the SLID/SLEND field, this field identifies the address of the coupled processor unit in the slave mode. In the master mode, this field identifies the last of the processors coupled to the interface unit. In the UPM field, field identifies whether a polling takes place in a round-robin manner or from a fixed address. The U16M field determines whether data transfers are 8 bits or 16 bits for both the input and the output interfaces. The MPHY field determines whether the interface unit is coupled to a single processor (logic "0") or to multiple processors. The ULB field determines whether the interface unit is in a loop-back mode. In the loop-back mode (i.e., logic "1"), the receive and transmit sections are coupled and the master is determined by the URMSTR/UXMSTR fields. The BEND field determines the data transfer in a big endian or little endian format.

[0045] Referring to FIG. 13, the operation of the (transmit) EVENT signal is illustrated. After initialization of the transmit portion of the UTOPIA interface unit in step 1300 or as part of the continuing operation of the interface unit, a determination is made in step 1301 whether a space for the storage of a complete data cell is available in the transmit buffer memory unit. When the determination is yes, then is step 1302 a transmit EVENT signal is applied to the direct memory access unit. In response to the generation of the EVENT signal, a data cell is transmitted through the direct memory access unit to the transmit buffer memory storage unit in step 1303. In step 1304, as soon as the transfer of the data cell has begun and the first word of the cell is written, the EVENT signal is cleared. Note that the EVENT signal is reasserted as soon as the first word is written and the buffer memory unit has space available. The immediate reassertion of the EVENT signal improves the interface unit throughput. The process then returned to step 1301 to determine whether space in the transmit buffer memory unit is available for storage of an entire data cell. When the determination is step 1301 is negative, the process returns to step 1301 and continues to cycle until space is available for the storage of an entire data cell.

[0046] Referring to FIG. 14, the operation of the event signal in the UTOPIA slave interface unit in the receive mode is illustrated. After initialization of the receive portion of the UTOPIA interface unit in step 1400 or as part of the operation of that portion of the interface unit, a determination is made whether a complete data cell is available in the receive buffer memory unit in step 1401. When the determination is yes, a receive EVENT signal is generated in step 1402. In response to the EVENT signal, the data cell in the receive buffer memory unit is transferred through the direct memory access unit in step 1403. In step 1404, as soon as the data cell transfer is begun with the reading of the first word, the EVENT signal is cleared. The process is then returned to step 1401 and is cycled until a complete data cell is stored in the receive buffer memory unit.

[0047] Referring to FIG. 15, the connection between a Utopia protocol slave state interface unit 18 of the present invention and an exemplary digital signal processing unit I/O unit 180 is illustrated. The timing diagram for the UTOPIA interface unit signals in the I/O transmit mode is shown in FIG. 16A, while the timing diagram for the UTOPIA interface signals in the I/O receive mode is shown in FIG. 16B. The I/O signals are typical of I/O devices, e.g., the Texas Instruments' Gigabit Transceiver. In the present invention, when the XVIO and the RVIO bits are set in the interface unit control register (cf. FIG. 12), the interface unit 18 is placed in the I/O mode and operates as an I/O device. The relationship between the signals can be understood as follows (wherein the parentheses indicate direction):

[0048] OUTDATA(out)/URDATA(in)=8-/16-digital data input to the Utopia interface unit

[0049] OUTCLK(out)/URCLK(in)=input clock provided by the I/O device

[0050] OUTDATAVALID(out)/URENB*(in)=data valid signal from I/O device, data on bus is valid only when this signal is active

[0051] OUTREADY(NA)/URENB(in)=cell available signal output from Utopia interface unit is equivalent to a READY signal, (not used in the TLK2500, but may be useful in other devices)

[0052] INDATA(in)/UXDATA(out)=8-/16-bit digital output from Utopia interface unit

[0053] INCLK(in)/UXCLK(in)=input clock provided by external source or I/O unit

[0054] INDATAVALID(in)/UXCLAV(out)=cell-available signal output from the Utopia interface unit is used to validate data, this signal should be driven active when UXENB* is active and valid data is on the bus.

[0055] INREADY(NA)/UXENB*(in)=data valid signal from the I/O device, data on this bus is valid only when the signal is active.

[0056] The function of the CLAV signal is different in the I/O mode as compared to the Utopia mode in the Utopia interface unit 18. The operation of the CLAV signal is independent of the state of the UXENB* signal. This operational mode means that, even before the port is enabled via the UXENB* signal, the data transmit queue will be available at the pins and the CLAV signal will be asserted. This feature is illustrated in the early part of FIG. 16A. The I/O device strobes the data based on the CLAV signal. During a transmit operation, if the UXENB* terminal is disabled by the I/O device, the data on the bus will be the last sent, and the next data is made available after the Utopia interface unit is enabled. This feature is illustrated by element 29 in FIG. 16A. When the transmit queue is empty, the UXCLAV signal is no longer asserted after driving the last data on the bus. The non-asserted UXCLAV signal means that the data on the bus is invalid. The UXCLAV signal will be asserted as soon as the first write to the buffer memory unit.

[0057] 2. Operation of the Preferred Embodiment

[0058] The asynchronous transfer mode interface unit of the present invention is the interface unit between the direct memory access unit and the data processing system. In general, all of the data processing units of a data processing system can include an asynchronous interface unit using the UTOPIA protocol that is coupled to a bus coupling the data processing units. In some implementations, the data processing unit itself can be implemented to provide the asynchronous transfer mode signals thereby obviating the need for the interface unit in that data processing system. The actual transfer of the data signals between data processing systems in the asynchronous transfer mode is under the control of the same clock or synchronized clock signals. The data cells or packets that have been transferred or that are to be transferred are stored in the buffer memory unit. The memory unit provides a buffer between the clock frequency of the communication bus and the much higher frequency of the direct memory access unit.

[0059] The foregoing description has described the interface unit as including a buffer memory unit. In the preferred embodiment, the buffer memory unit is implemented by a first-in/first out memory unit. The memory unit is provided with the capacity to store two data cells. The communication bus causes

the signals to be exchanged between the master unit and the slave unit to have a relatively slow clock speed. Because of the relatively slow clock speed of the communication bus, the filling or emptying of the buffer memory in the direction of the communication will be much slower than the filling and the emptying of the buffer memory unit in the direction of the direct access memory unit. Similarly, although the direct memory access unit can handle only one data transfer at a time, because of the difference in clock speed between the communication bus and the processing unit of which the direct memory access unit is a part

[0060] The EVENT signal is particularly useful in the efficient transfer of data cells. Because the operation of the data processing system of which the UTOPIA interface is a part is much faster than the rate at which data can be transferred over the communication bus, the transfer of data cells out of the transmit buffer memory unit and into the receive buffer memory unit can be essentially continuous.

[0061] While one important application of the present invention is the transfer of data signals between a host or master-state data processing unit (that includes a microprocessor) and at least one slave-state data processing unit (that typically includes a digital signal processor), this configuration can be reversed. In addition, the UTOPIA transfer mode interface unit can be added to each or a series of digital signal processing units coupled by a bus. One of the digital signal processing unit is selected as being the master-state machine and this processing unit controls the operation of all the digital signal processors.

[0062] The Utopia interface unit identifies the transfer of an incomplete ATM cell, sometimes referred to as a runt cell, when the SOC signal is set during a ATM cell transfer. In the software resolution, the runt cell can be resolved by transferring the runt cell to a higher level software procedure. In the preferred embodiment, the runt cell is overwritten by new data under hardware control.

[0063] By proper interpretation of the signals exchanged with the communication bus, the UTOPIA ATM interface unit of the present invention can function as an I/O interface unit. This versatility permits a single interface unit to be fabricated on an integrated circuit chip in association with a digital signal processing unit to act in either interface capacity. The single interface unit's results in decrease in size and complexity of the integrated circuit when compared to fabricating each of the interface units in the integrated circuit.

[0064] While the invention has been described with respect to the embodiments set forth above, the invention is not necessarily limited to these embodiments. Accordingly, other embodiments, variations, and improvements not described herein are not necessarily excluded from the scope of the invention, the scope of the invention being defined by the following claims.

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